UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/725,888	02/04/2004	William J. Borland	EL0497USNA	3392

23906 7590 11/02/2006

E I DU PONT DE NEMOURS AND COMPANY
LEGAL PATENT RECORDS CENTER
BARLEY MILL PLAZA 25/1128
4417 LANCASTER PIKE
WILMINGTON, DE 19805

EXAMINER	
NGUYEN, HOA CAO	

ART UNIT	PAPER NUMBER
2841	

DATE MAILED: 11/02/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/725,888	BORLAND ET AL.	
	Examiner	Art Unit	
	Hoa C. Nguyen	2841	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *09 August 2006*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-30* is/are pending in the application.

4a) Of the above claim(s) *6-30* is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-5* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

1. Claims 6-30 withdrawn from further consideration pursuant to 37 CFR 1.142(b) as being drawn to a nonelected group, there being no allowable generic or linking claim. Election was made **without** traverse in the reply filed on 8/9/06.

Claim Objection

2. The amended claim 2 is approved. The objection to claim 2 is withdrawn.

Claim Rejections - 35 USC § 102

3. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

4. Claims 1-5 are rejected under 35 U.S.C. 102(e) as being anticipated by Nakano et al. (US 6785121).

Regarding claim 1, as shown in figure 1, Nakano et al. disclose a printed wiring board, comprising:

(a) A first innerlayer panel (any number of layers shown in the figure can be arbitrary group into a panel - all dielectric layer and electrodes are denoted by reference characters 2 and 3 respectively), the first innerlayer panel (considering the bottom layers as a first innerlayer panel) comprising:

(b) a first electrode 3 (considering the first electrode 3 from the bottom of the stack shown in the figure), see column 3, lines 28-48;

(c) a dielectric 2 (considering the dielectric disposed on top of the first electrode) disposed over the first electrode 3;

(d) a second electrode 3 (considering the electrode on top of the first one spaced apart by a dielectric layer) disposed over the dielectric,

(c) the first electrode, the dielectric and the second electrode form a first capacitor (noticed: a pair of conductive layers sandwiches a thin layer of dielectric material inherently forms a capacitor);

(e) a second innerlayer panel (any number of layers formed on top of the above capacitor can be arbitrary group into a panel), the second innerlayer panel comprising:

(f) A first electrode 3;

(g) a dielectric 2 disposed over the first electrode;

(h) a second electrode 3 disposed over the dielectric,

(i) the first electrode, the dielectric and the second electrode form a second capacitor,

(j) the second innerlayer panel is stacked with the first innerlayer panel, the respective first electrodes are electrically coupled through a conductive via (no number - to form one of external electrodes 4), and the respective second electrodes are electrically coupled through a conductive via (no number - to form another external electrode 4), thereby connecting the first and second capacitors in parallel.

It is noticed that Nakano et al. disclose a plurality of dielectric and electrode layers formed parallel on top of each other. Any group of layering structure with dielectric layers sandwiched between at least two conductive layers conventionally formed a capacitor. The capacitors are stacked on each other and connected in parallel forming a larger storage capacitor. In one of examples, Nakano et al. disclose a stacked capacitor with electrodes formed on a stack of 100 layers of dielectric material, see column 8, lines 63-66.

Regarding claim 2, as shown in figure 1, Nakano et al. disclose every limitation as shown in claim 1 above inherently including a third capacitor, fourth capacitor, fifth capacitor, ..ect.., stacked on top of each other and electrically connected in parallel.

Regarding claim 3, as shown in figure 1, Nakano et al. disclose every limitation as shown in claim 1 above including a third electrode spaced from the second electrode by the dielectric and electrically coupled to the first electrode, wherein the dielectric is a two-layer dielectric.

Regarding claim 4, as shown in figure 1, Nakano et al. disclose every limitation as shown in claims 1 and 3 above including a fourth electrode spaced from the third electrode by the dielectric and electrically coupled to the second electrode, wherein the dielectric is a three-layer dielectric.

Regarding claim 5, as clearly shown in figure 1, Nakano et al. disclose the respective first and second electrodes are electrically coupled by a first and second conductive via (no number, conductive vias for external electrodes 4 for external connections).

Response to Arguments

5. Applicants' arguments filed 4/17/06 have been fully considered but they are not persuasive.

Remarks, pages 10-11: Applicants' arguments is centering about the different between the structure of capacitors of the claimed invention and of the prior reference art (US 6785121), in which the claimed invention teaches a stack of fired-on-foil capacitors embedded within an organic medium of a printed wiring board, while the prior reference art does not teach such fired-on-foil capacitors embedded in such organic medium.

The arguments are not persuasive, because the claims fail to recite any structure limitation with the regard to the stack of fired-on-foil capacitors embedded within the organic medium of a circuit board that would keep the claims from reading on the interpretation of the prior reference art which also discloses a stack of capacitors, wherein each capacitor also has a dielectric substrate formed in between a pair of electrodes.

Conclusion

6. **THIS ACTION IS MADE FINAL.** Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the

shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

7. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Hoa C. Nguyen whose telephone number is 571-272-8293. The examiner can normally be reached on M-F.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Riechard Dean can be reached on 571-272-1984. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Hoa C. Nguyen
10/15/06

Dean A. Reichard 10/30/06

DEAN A. REICHARD
SUPERVISORY PATENT EXAMINER
TECHNOLOGY CENTER 2800